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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/966,481	09/28/2001	Nathan Y. Moyal	INTL-0552-US (P11111)	6467
21906	7590	10/24/2003	EXAMINER	
TROP PRUNER & HU, PC 8554 KATY FREEWAY SUITE 100 HOUSTON, TX 77024			NGUYEN, HAI L	
			ART UNIT	PAPER NUMBER
			2816	

DATE MAILED: 10/24/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/966,481

Applicant(s)

MOYAL, NATHAN Y.

Examiner

Hai L. Nguyen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 04 August 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 11-13, 16-18, 20 and 44-46 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 11-13, 16-18, 20 and 44-46 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 28 September 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## **DETAILED ACTION**

### ***Response to Amendment***

1. The amendment received on 08/04/03 has been reviewed and considered with the following results:

As to the objections to claim 11, Applicant's amendments have overcome the objections, as such; the objections have been withdrawn.

As to the rejections to the claims, under 35 U.S.C. 112, 2nd paragraph, Applicant's amendments have overcome the rejections, as such; the rejections have been withdrawn.

As to the prior art rejections to the claims, the arguments and/or comments by the applicant have been carefully reviewed, but are not persuasive. A new action on the merits appears below in view of Applicant's amendments to the claims.

The response to Applicant's arguments is addressed as set forth below.

### ***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 11, 13, 16-18, 20, 44, and 45 are rejected under 35 U.S.C. 102(b) as being anticipated by Shay (US 5,323,067; previously cited).

With regard to claims 11, Shay discloses in Fig.1 an integrated circuit comprising an activation circuit (12, 14, 16, 50, 62, 76) to determine whether a supply voltage (VDD) reaches a

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predetermined level, the activation circuit including an inverter (76) coupled to the gate of a load transistor (64), a second transistor (66) coupled to the load transistor and a third transistor (60) coupled between the load transistor and the second transistor; a pulse generator (68, 70, 72, 74) to generate pulses (38, 40) to indicate that the supply voltage is ramping up and to terminate the generation of the pulses after the supply voltage reaches a predetermined level (see column 4, line 16 through column 5, lines 33); and a feedback path provide an output of the pulse generator to the activation circuit, the activation circuit to latch a high in response to a low signal on the feedback path (note 38 is High in response to a low on node 30).

With regard to claim 13, the integrated circuit includes a level detector (14) that detects when a voltage is above at least two transistor threshold voltages, the level detector operative to control the pulse generator (column 4, line 6 through column 5, line 13).

With regard to claim 16, the integrated circuit includes a pair of transistors (68, 70) that must both conduct in order to generate the pulse.

With regard to claim 17, the integrated circuit includes a capacitor circuit (64) to enable the supply voltage to reach a designated output level (see column 5, lines 14-33).

With regard to claim 18, the integrated circuit includes a hysteresis sense stage (58, 60) coupled to the capacitor circuit (see column 4, line 27 through column 5, line 13).

With regard to claim 20, the integrated circuit includes a circuit (18) to latch the pulse generator in response to the supply voltage being in a first state.

With regard to claim 44, the load transistor (64) is coupled to the supply voltage (20).

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With regard to claim 45, the integrated circuit further includes a second activation circuit (80) to determined whether the supply voltage reaches the predetermined level (see column 5, lines 34-54).

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shay in view of Ansel et al. (US 5,809,312; previously cited).

The above discussed the integrated circuit of Shay meets all of the claimed limitations except for a logic functionality (52 in instant Fig.5) to emulate logic that is difficult to trigger and to determine whether the supply voltage has reached a level sufficient to trigger the difficult to trigger logic. Ansel et al. teaches in Fig.3 a circuit having a logic functionality (310) as recited in the claim. Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention was made to utilize that logic functionality taught by Ansel et al. with the prior art (Fig.1 of Shay) in order to ensure all of the critical integrated circuits are operating correctly.

6. Claim 46 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shay in view of Wu et al. (US 6,288,584).

With regard to claim 46, the above discussed the integrated circuit of Shay meets all of the claimed limitations except for the limitation that the capacitor circuit includes a first capacitor coupled to the supply voltage and a second capacitor coupled to the first capacitor through a transistor. Wu et al. teaches in Fig.3 an integrated circuit having a capacitor circuit (100, 102) that includes a first capacitor (14) coupled to the supply voltage and a second capacitor (16) coupled to the first capacitor through a transistor (30) as recited in the claim. Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention was made to utilize that teaching of Wu et al. with the prior art (Fig.5 of Shay et al.) for the advantage of saving power by not drawing current either on the standby mode or after the supply voltage reaches the predetermined level,

### ***Response to Arguments***

7. Applicant's first argument is that "The Office Action states that in Shay an inverter 76 is coupled to the gate of a load transistor. Office Action, page 3. However, transistor 76 is a latching transistor, not an inverter" is not persuasive because element 76 (Shay's Fig.1) is inherently an inverter since it does generate an output signal (node 30) which is a complement of an input signal (node 38). Even though, Shay calls it under a different name, it still has a functional of an inverter. Therefore, by given the broadest reasonable interpretation, element 76 is an inverter.

8. Applicant's second argument is that "the Office Action indicates that transistors 68, 70, 72, 74 of Shay generate pulses to indicate that a supply voltage is ramping up and to terminate pulse generation after the supply voltage reaches a predetermined level. However, these

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transistors are an inverter, not a pulse generator. Shay, 3:55-60. Thus, this inverter does not act as a pulse generator” is not persuasive because those elements clearly are a pulse generator since it does generate a low pulse output signal (at node 38) to indicate that a supply voltage is ramping up and to terminate pulse generation after the supply voltage reaches a predetermined level (see column 4 line 16 through column 5 line 9). Even though, Shay does not disclose those elements are a pulse generator, it still has a functional of a pulse generator. Therefore, by given the broadest reasonable interpretation, those elements are a pulse generator.

9. Applicant’s last argument is that “Nor does Shay include an activation circuit that latches a high signal in response to a low signal on a feedback path” is not persuasive because the disclosure (see column 6 lines 21-28) clearly describes that the activation circuit latches a high signal (at node 38) in response to a low signal (at node 30) on a feedback path.

Therefore, the rejections to those claims are proper and remain as set forth above.

### *Conclusion*

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a).

Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37


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CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hai L. Nguyen whose telephone number is 703-306-9178 and Right Fax number is 703-746-3951. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 703-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

HLN   
October 17, 2003

  
TIMOTHY P. CALLAHAN  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2800